AMENDMENTS

In the title

Please change title to read as follows: --SCHEDULER FOR A DIRECT MEMORY ACCESS DEVICE HAVING MULTIPLE CHANNELS--.

In the specification

On page 1, please replace the paragraph beginning on line 6 with the following revised paragraph:

--The present ~~invention~~ application generally relates to a scheduler and more particularly to a scheduler for a [[Data]] Direct Memory Access (DMA) device having multiple channels.--

On page 1, please replace the paragraph beginning on line 9 with the following revised paragraph:

--In general, the [[Data]] Direct Memory Access (DMA) of a device controls the transfer of data between peripheral devices and the memory of the device. The device may include an input DMA and an output DMA to service data received from peripheral devices and data sent to peripheral devices, respectively. When a peripheral device wants to send data to a device with an input DMA, the peripheral device sends a request to the input DMA. The input DMA can then send an Acknowledgement (ACK) to the peripheral. When the peripheral device receives the ACK, it transfers data to the input DMA, which then transfers the data into memory. When data is to be sent out to a peripheral device, the processor of the device sends a request to the output DMA. The output DMA then retrieves data from memory and sends it out to the peripheral device.--

On page 2, please replace the paragraph beginning on line 2 with the following revised paragraph:

--The present invention relates to a scheduler for scheduling multiple channels of a [[Data]] Direct Memory Access (DMA) device. In accordance with one aspect of the present invention, a scheduler includes a shift structure having entries corresponding to the multiple channels to be scheduled. Each entry in the shift structure includes multiple fields. Each entry also includes a

weight that is determined based on these multiple fields. The scheduler also includes a comparison-logic circuit that is configured to then sort the entries based on their respective weights.--

On page 3, please replace the paragraph beginning on line 22 with the following revised paragraph:

--As described above, line card 100 can receive various types of signals. Line card 100 can also receive mixed signals, such as a mix of circuit-switched signals and packet signals. As such, [[line]] framer ASIC 104 can be configured to separate packet signals, then pass them onto PPAs 106 for processing.--

On page 6, please replace the paragraph beginning on line 17 with the following revised paragraph:

--As described above, when input DMA 204 receives a packet, it stores the packet in memory. More particularly, input DMA 204 obtains from FMG 210 free MDUs to store the packet in memory. Accordingly, FMG 210 is configured to keep track of which MDUs are free and which are being used. As described earlier, an MDU is 256-bytes long. If a packet is longer than 256-bytes, then input DMA 204 allocates the appropriate number of additional MDUs to store the packet. Input DMA 204 then creates a link list of MDUs. For a more detailed description of output FMG 210 see U.S. Patent Application Serial No. 09/740,670 ~~NN/NNN,NNN~~, entitled "Free Memory Manager Scheme and Cache", filed on December 18, 2000, the entire content of which is incorporated by reference.--

On page 7, please replace the paragraph beginning on line 10 with the following revised paragraph:

--As described above, EUs 214 retrieve the stored packet and process it. More particularly, EUs 214 read a descriptor out of input-descriptor queue 206. EUs 214 then retrieve the packet from memory using the descriptor. For example, EUs 214 can read the descriptor for a pointer to the first MDU containing the packet. EUs 214 can read the header of the packet, parse it, and classify the packet. EUs 214 can then modify certain fields of the packet before sending out the packet. In one embodiment of the present invention, EUs 214 include 16 Reduced Instruction Set Computer (RISC) processors. For a more detailed description of output EUs 214 see U.S. Patent Application Serial No. 09/740,658 ~~NN/NNN,NNN~~, entitled "Cache ~~Request Retry~~ Retry Request Queue", filed on December 18, 2000, the entire content of which is incorporated by reference. It should be recognized, however, that EUs 214 can include any number and types of processors. Additionally, it should be recognized that EUs 214 can execute various software programs to process the packets in various manner.--

On page 10, please replace the paragraph beginning on line 13 with the following revised paragraph:

--As depicted in Fig. 4, LOP 216 includes four PSFs 308 (i.e., PSFs 308-0 to 308-3). In the present embodiment, each PSF 308 can be configured to service up to 16 channels. However, in the configuration depicted in Fig. 4, PSFs 308-0 and 308-2 are configured to service up to 16 channels, but PSFs 308-1 and 308-3 are configured to service up to 8 channels. More particularly, PSF 308-0 is configured to service channels 0 to 15. As such, PSF 308-0 is connected to LSPs 306-0, 306-1, 306-2, and 306-3. PSF 308-1 is configured to service channels 8 to 15. As such, PSF 308-1 is connected to LSPs 306-2 and 306-3. It should be recognized, however, that PSF [[306-1]] 308-1 can be configured to service channels 0 to 15 by connecting it to LSPs 306-0 and 306-1. PSF 308-2

is configured to service channels 16 to 31. As such, PSF 308-2 is connected to LSPs 306-4, 306-5, 306-6, and 306-7. PSF 308-3 is configured to service channels 24 to 31. As such, PSF 308-3 is connected to LSPs 306-6 and 306-7. It should be recognized, however, that PSF [[306-3]] 308-3 can be configured to service channels 16 to 31 by connecting it to LSPs 306-4 and 306-5. It should be recognized that LOP 216 can include any number of PSFs 308. It should be recognized that PSF 308 can be configured to service any number of channels and connected to any number of LSTs 306. It should be further recognized that PSFs 308 can be mapped to LSTs 306 using various mapping schemes. Moreover, this mapping scheme can be altered either through hardware and/or software.--